

High voltage fast-switching NPN power transistor

Features

- High voltage capability
- Low spread of dynamic parameters
- Minimum lot-to-lot spread for reliable operation
- Very high switching speed

Applications

- Compact fluorescent lamp (CFL)
- Switch mode power supplies (AC/DC converters)

Description

The device is manufactured using high voltage Multi-Epitaxial Planar technology for high switching speeds and medium voltage capability. It uses a cellular emitter structure with planar edge termination to enhance switching speeds while maintaining the wide RBSOA.

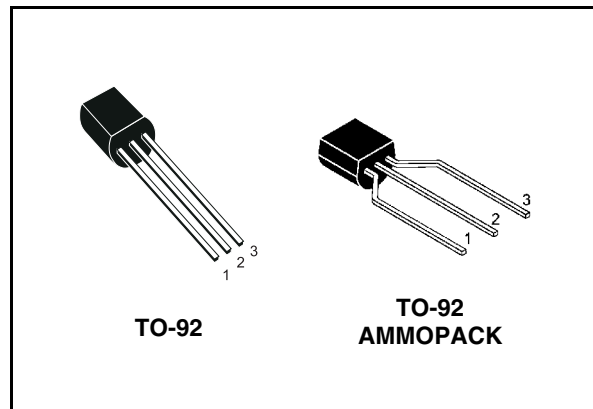


Figure 1. Internal schematic diagram

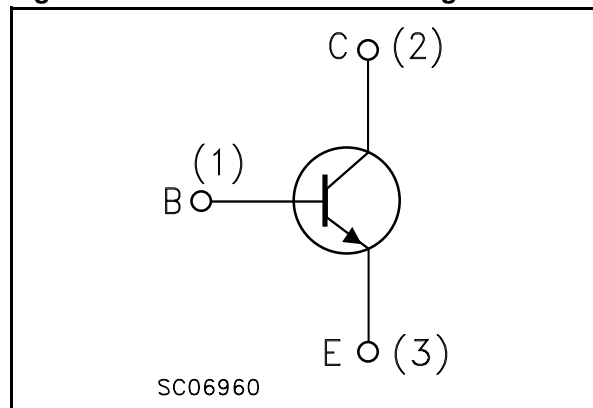


Table 1. Device summary

Order code	Marking	Package	Packaging
STX13005	X13005	TO-92	Bulk
STX13005-AP	X13005	TO-92	Ammopack

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1 Electrical ratings

Table 2. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{BE} = 0$)	700	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	400	V
V_{EBO}	Emitter-base voltage ($I_C = 0$; $I_B = 1.5$ A; $t_p < 10$ ms)	$V_{(BR)EBO}$	V
I_C	Collector current	3	A
I_{CM}	Collector peak current ($t_p < 5$ ms)	6	A
I_B	Base current	1.5	A
I_{BM}	Base peak current ($t_p < 5$ ms)	3	A
P_{tot}	Total dissipation at $T_C = 25^\circ\text{C}$	2.8	W
T_{stg}	Storage temperature	-65 to 150	$^\circ\text{C}$
T_J	Max. operating junction temperature	150	$^\circ\text{C}$

2 Electrical characteristics

($T_{\text{case}} = 25^{\circ}\text{C}$ unless otherwise specified)

Table 3. Electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector cut-off current ($V_{\text{BE}} = 0$)	$V_{\text{CE}} = 700 \text{ V}$			1	mA
		$V_{\text{CE}} = 700 \text{ V}$ $T_{\text{C}} = 125^{\circ}\text{C}$			5	mA
I_{CEO}	Collector-cut-off current ($I_{\text{B}} = 0$)	$V_{\text{CE}} = 400 \text{ V}$			1	mA
$V_{(\text{BR})\text{EBO}}$	Emitter base breakdown voltage ($I_{\text{C}} = 0$)	$I_{\text{E}} = 10 \text{ mA}$	9		18	V
$V_{\text{CEO(sus)}}^{(1)}$	Collector-emitter sustaining voltage ($I_{\text{B}} = 0$)	$I_{\text{C}} = 10 \text{ mA}$	400			V
$V_{\text{CE(sat)}}^{(1)}$	Collector-emitter saturation voltage	$I_{\text{C}} = 1 \text{ A}$ $I_{\text{B}} = 200 \text{ mA}$			0.5	V
		$I_{\text{C}} = 2 \text{ A}$ $I_{\text{B}} = 500 \text{ mA}$			0.6	V
		$I_{\text{C}} = 3 \text{ A}$ $I_{\text{B}} = 750 \text{ mA}$			5	V
$V_{\text{BE(sat)}}^{(1)}$	Base-emitter saturation voltage	$I_{\text{C}} = 1 \text{ A}$ $I_{\text{B}} = 200 \text{ mA}$			1.2	V
		$I_{\text{C}} = 2 \text{ A}$ $I_{\text{B}} = 500 \text{ mA}$			1.6	V
$h_{\text{FE}}^{(1)}$	DC current gain	$I_{\text{C}} = 1 \text{ A}$ $V_{\text{CE}} = 5 \text{ V}$	10		30	
		$I_{\text{C}} = 2 \text{ A}$ $V_{\text{CE}} = 5 \text{ V}$	8		24	
t_{s} t_{f}	Resistive load Storage time	$I_{\text{C}} = 2 \text{ A}$ $V_{\text{CC}} = 125 \text{ V}$ $I_{\text{B1}} = -I_{\text{B2}} = 400 \text{ mA}$		1.65		μs
	Fall time	$t_{\text{p}} = 30 \mu\text{s}$		260		ns
t_{s} t_{f}	Inductive load Storage time	$I_{\text{C}} = 1 \text{ A}$ $V_{\text{clamp}} = 300 \text{ V}$ $I_{\text{B1}} = 200 \text{ mA}$ $V_{\text{BE(off)}} = -5 \text{ V}$		0.8		μs
	Fall time	$L = 50 \text{ mH}$ $R_{\text{BB}} = 0$		150		ns

1. Pulsed duration = 300 ms, duty cycle $\leq 1.5\%$

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

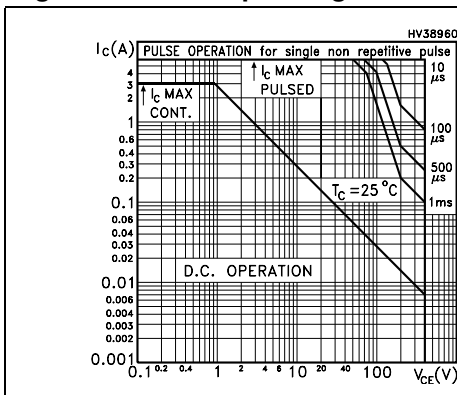


Figure 3. Safe operating area

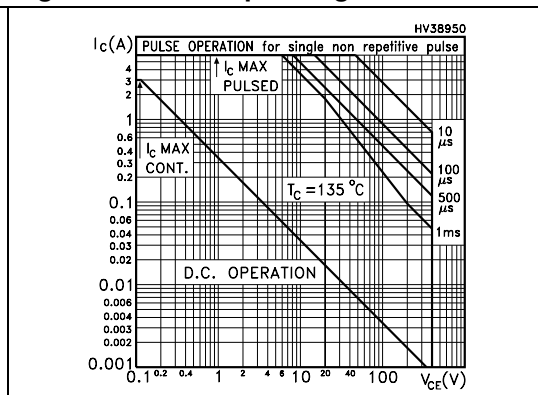


Figure 4. Derating curve

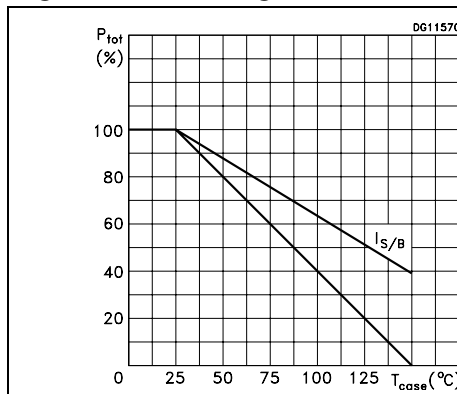


Figure 5. Output characteristics

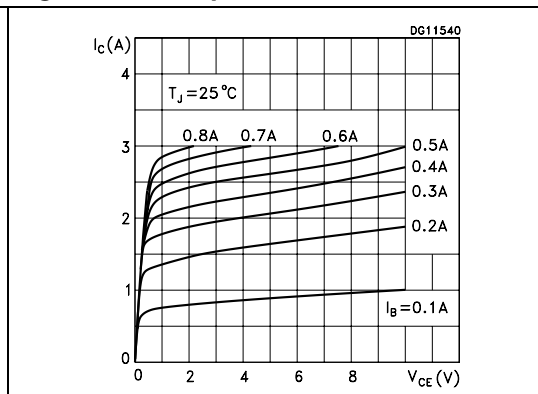


Figure 6. DC Current Gain

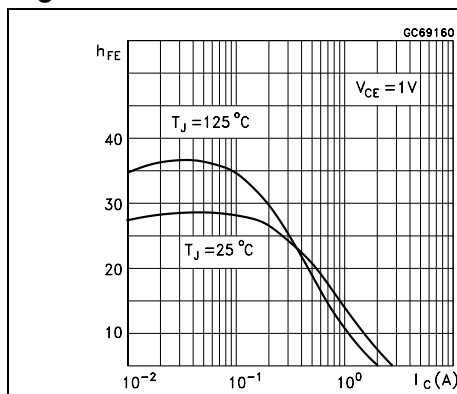


Figure 7. DC Current Gain

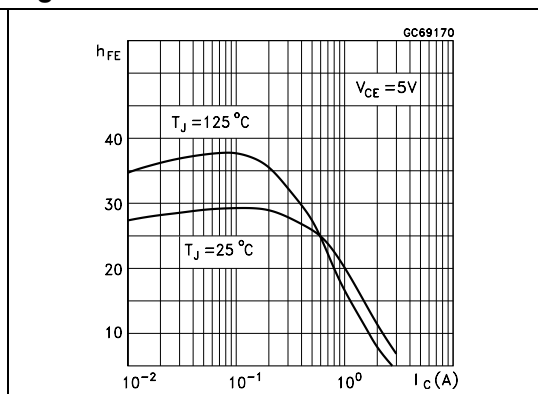


Figure 8. Collector-emitter saturation voltage

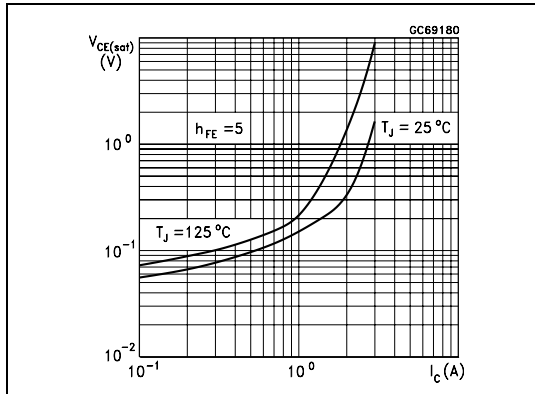


Figure 9. Base-emitter saturation voltage

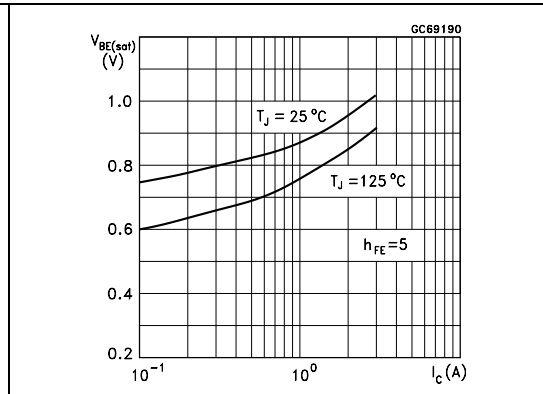


Figure 10. Inductive load fall time

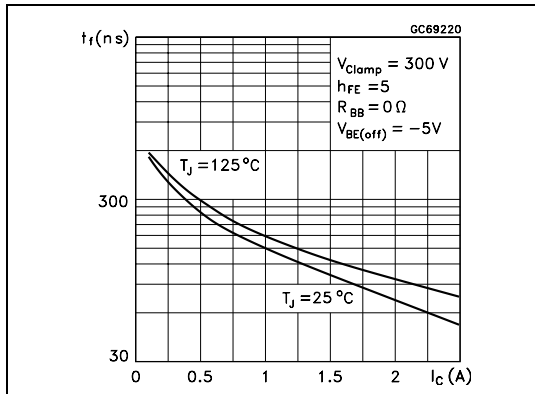


Figure 11. Inductive load storage time

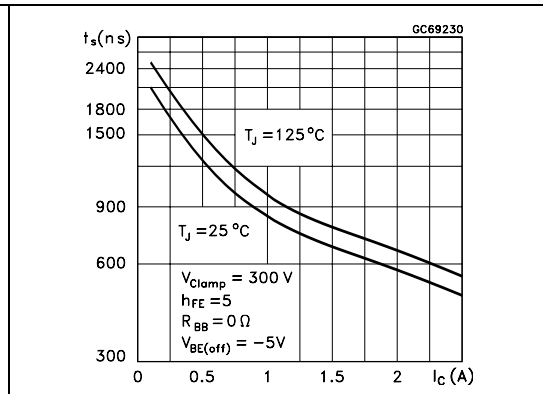


Figure 12. Resistive load fall time

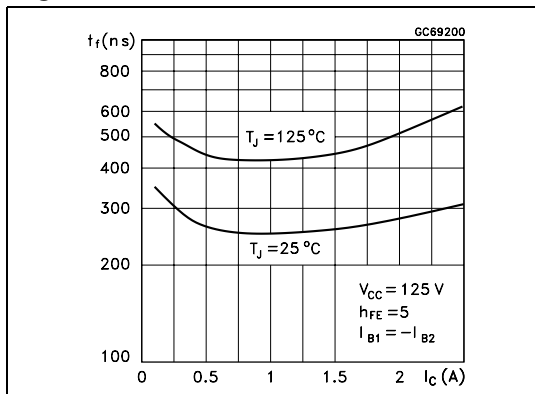


Figure 13. Resistive load storage time

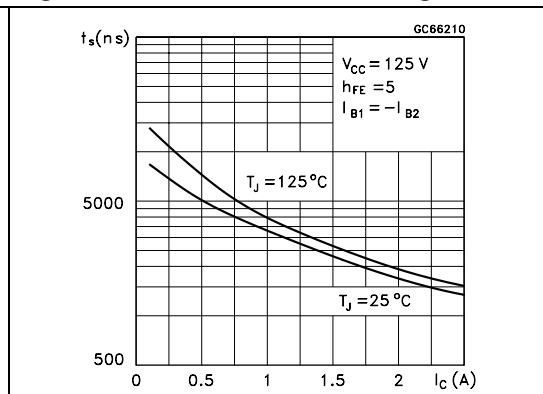
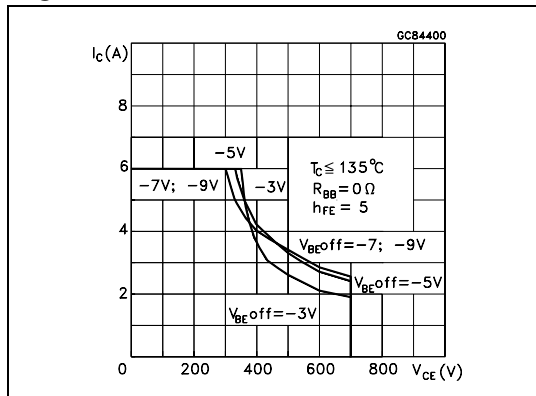


Figure 14. Reverse biased SOA



3 Test circuit

Figure 15. Inductive load switching test circuit

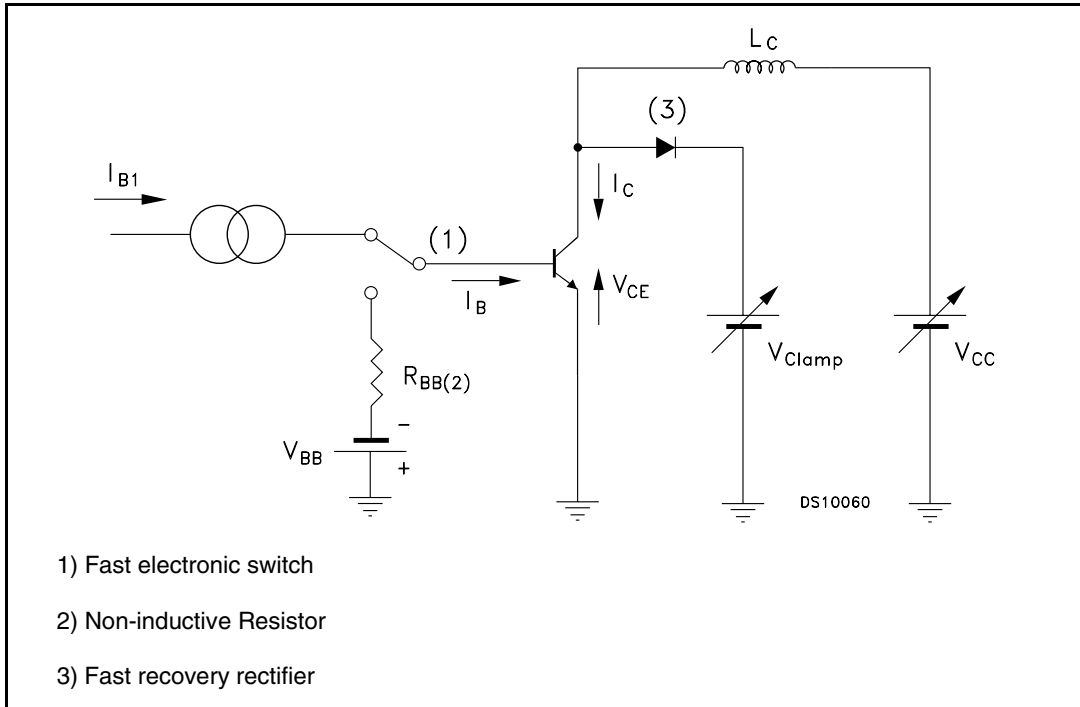
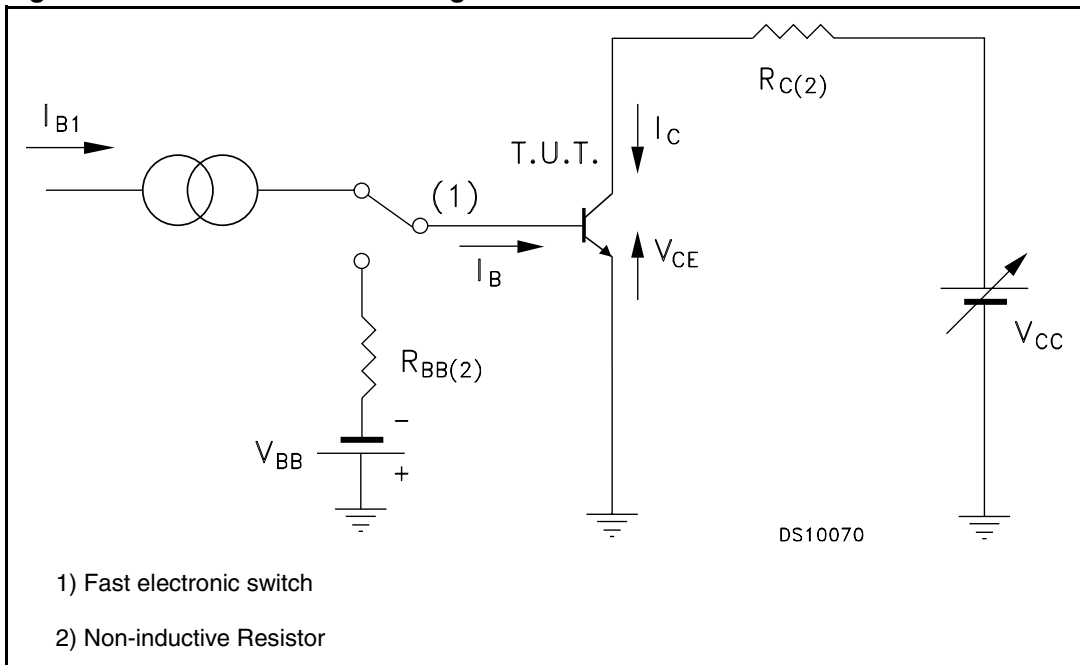


Figure 16. Resistive load switching test circuit

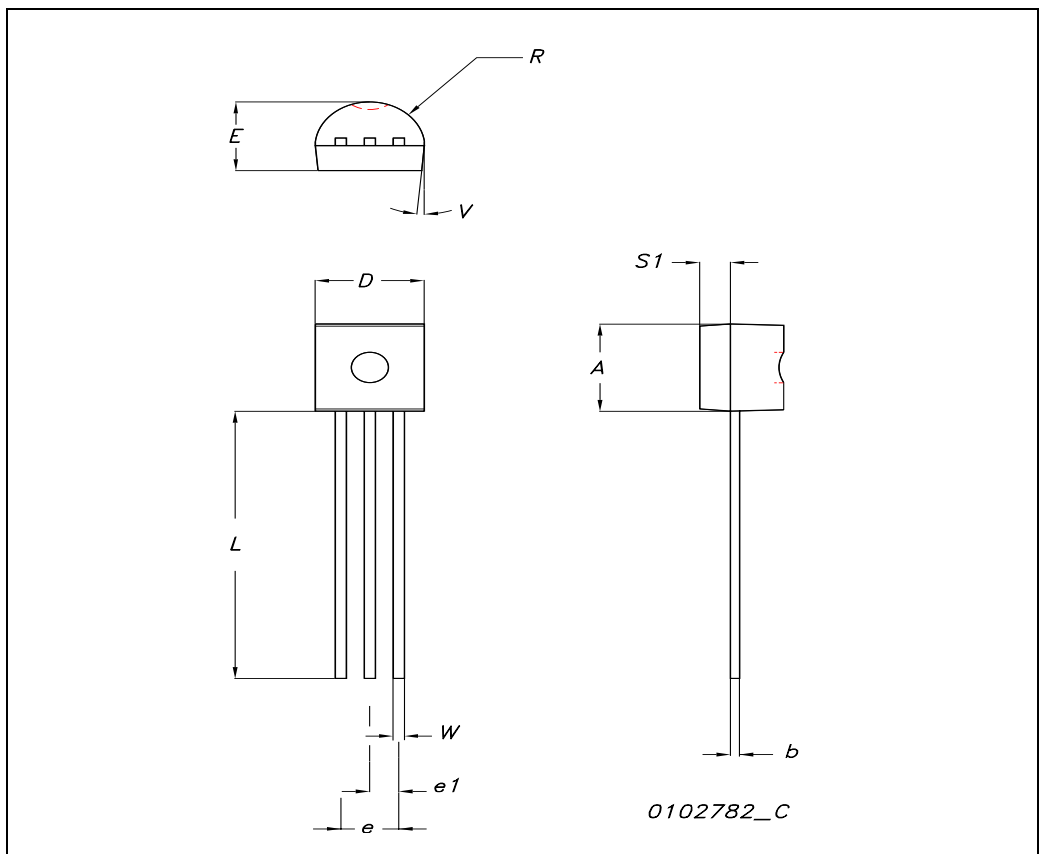


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

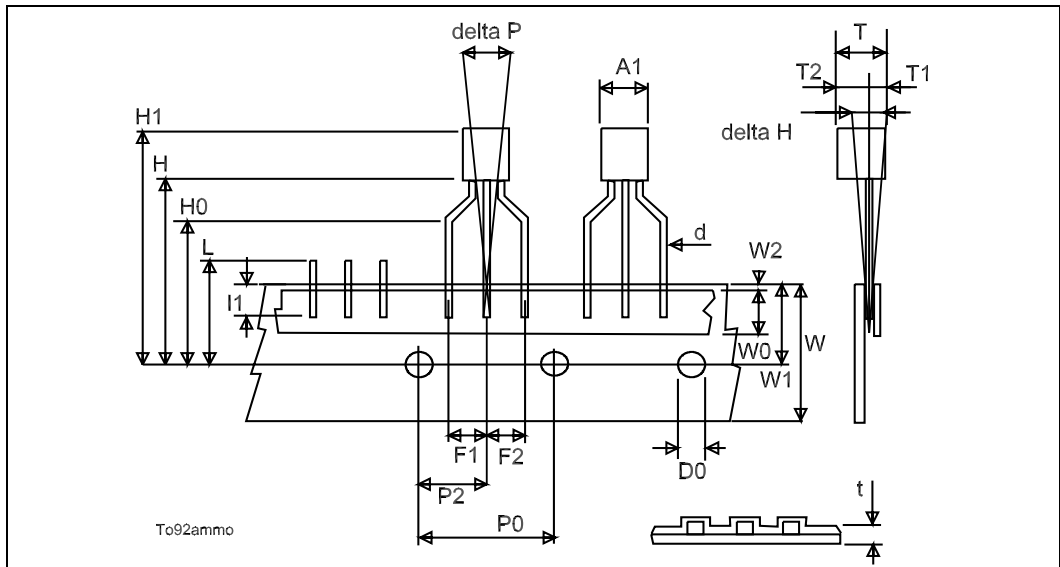
TO-92 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°	



TO-92 AMMOPACK

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A1	4.45		4.95	0.170		0.194
T	3.30		3.94	0.130		0.155
T1			1.6			0.06
T2			2.3			0.09
d	0.41		0.56	0.016		0.022
P0	12.5	12.7	12.9	0.49	0.5	0.51
P2	5.65	6.35	7.05	0.22	0.25	0.27
F1, F2	2.44	2.54	2.94	0.09	0.1	0.11
delta H	-2		2	-0.08		0.08
W	17.5	18	19	0.69	0.71	0.74
W0	5.7	6	6.3	0.22	0.23	0.24
W1	8.5	9	9.25	0.33	0.35	0.36
W2			0.5			0.02
H	18.5		20.5	0.72		0.80
H0	15.5	16	16.5	0.61	0.63	0.65
H1			25			0.98
D0	3.8	4	4.2	0.15	0.157	0.16
t			0.9			0.035
L			11			0.43
l1	3			0.11		
delta P	-1		1	-0.04		0.04



5 Revision history

Table 4. Document revision history

Date	Revision	Changes
01-Jul-2004	1	First release.
11-Feb-2005	2	New table on page 1
02-Aug-2007	3	New <i>Figure 3</i> and updated <i>Figure 14</i>
28-Sep-2007	4	Updated <i>Figure 2</i> and <i>Figure 3</i>

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